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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,999	02/16/2001	Jay E. Uglow	LAMP1P106A	2171

25920 7590 07/07/2005

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	09/785,999	UGLOW ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9 and 33-35* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 29 April 2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,197,696 B1 (**Aoi**).

Regarding **claims 1, 4 and 35**, **Aoi** discloses a method for malting a dielectric structure for dual damascene applications, the method comprising:

(a) providing a substrate **350** (Fig. 15(a));

(b) fabricating a first metallization metallization lines **351** in the substrate **350** (Fig. 15(a));

(c) forming a barrier layer **352** of silicon nitride (col. 19, lines 1-2) --as further limited by instant **claim 4**-- over the first metallization lines **351** and the substrate **350** (Fig. 15(a));

(d) forming an inter-metal dielectric structure, the forming of the inter-metal dielectric structure **consisting of**:

(d)(i) forming an inorganic dielectric layer **353** of silicon dioxide (col. 19, lines 3-5) to define a via dielectric layer **353A** directly over the barrier layer **352**, the inorganic dielectric

layer **353** having a dielectric constant of about 4 (col. 1, lines 53-54) --as further limited by instant **claim 35**-- and being highly selective relative to the barrier layer **352** when etched (as shown in Fig. 16(c)); and

(d)(ii) forming a carbon doped oxide layer **354** (called "organic layer" at col. 19, lines 6-8) to define a trench dielectric layer **354A** that is defined directly over and in direct contact with the inorganic dielectric layer **353**, the trench layer **354** being formed to define a metallization line layer **365** (Fig. 16(d) and 17(c));

(d)(iii) forming a trench **360**, **362** in the carbon doped oxide layer using a first etch chemistry (Fig. 16(d); col. 19, lines 50-62); and

(d)(iv) forming a via **361** in the inorganic dielectric layer **353** from within the trench **360**, **362** using a second etch chemistry, the second etch chemistry being different than the first etch chemistry (col. 19, lines 41-62).

Note that **Aoi** defines "organic layer" to include carbon-doped oxides (called "organic-containing silicon dioxide") such as formed by CVD from precursors such as hexamethyldisiloxane, arylalkoxy silane, etcetera at col. 10, lines 54-62.

(See section entitled, "Modified Example of Embodiment 3" beginning in col. 18, line 60 for details of the embodiment used above from **Aoi** to reject the claim 1.)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoi** in view of US 6,110,648 (**Jang**).

Aoi teaches **exemplary** thicknesses of the via **353A** and trench **354A** dielectric layers of 1 μm and 0.4 μm, respectively (Aoi, col. 19, lines 4-8). **Aoi** does not teach via dielectric layer thicknesses of 0.4 to 0.5 μm and trench dielectric layer thicknesses of 0.5 to 0.6 μm.

Jang --like **Aoi**-- teaches a dual damascene process wherein the via **120a** and trench **120b** dielectric layers are made of different dielectric layers including an oxide and a low-k dielectric. Accordingly **Jang** and **Aoi** are drawn to the same field of endeavor. The thickness of the via dielectric layer **120a** is 0.5 μm to 0.8 μm (5000 Å to 8000 Å), and the thickness of the trench dielectric layer **120b** is 0.5 μm to 0.8 μm (5000 Å to 9000 Å), which overlap the claimed ranges. Moreover, it is noted that the instant specification indicates that the thicknesses are exemplary. Accordingly, there exists no evidence of record indicating that the thicknesses are critical. **Aoi** also indicates that the thicknesses are exemplary.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the dielectric layer thicknesses of **Jang** as the thicknesses in **Aoi** in order to use less of the high-k, via dielectric layer **353A** (1 μm in the example in **Aoi** but 0.5 μm to 0.8 μm in **Jang**), thereby reducing the overall dielectric constant of the ILD which reduces the RC delay and increases signal speed. A faster semiconductor device results.

Further in this regard it has been held,

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart

> patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... **More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.**" *In re Aller* 105 USPQ233, 255 (CCPA 1955). (Emphasis added.)

See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmscher* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sold* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

5. Claims 5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoi** in view of the basic text of **Wolf**, et al. Silicon Processing for the VLSI Era, Vol. 2-Process Integration, Lattice Press: Sunset Beach CA, 1990, p. 194.

Regarding **claims 5, 7, and 8**, the prior art of **Aoi**, as explained above, discloses each of the claimed features except for indicating that the silicon dioxide layer **353** is made from TEOS. **Aoi** does however state,

> "The first and second silicon dioxide films **353** and 355 may be deposited by **any arbitrary technique**. For example, these films 353 and 355 may be deposited **by a CVD process** using a reactive gas mainly composed of phenyltrimethoxy silane." (Emphasis added. Aoi, col. 19, lines 13-17.)

Wolf teaches that it is notoriously well-known in the art to form silicon dioxide using CVD from TEOS for forming dielectric films for multi-level interconnect metallization (p. 194), such as in the multilevel interconnect metallization of **Aoi**.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use TEOS to form the silicon dioxide layer **353** of **Aoi**, because **Aoi** teaches that any arbitrary method and particularly CVD can be used and **Wolf** teaches TEOS is known for making silicon dioxide for multi-level metallization.

Further regarding **claim 8**, **Aoi** discloses a method for making a dielectric structure for dual-damascene applications as recited in claim 7, wherein the first etch chemistry is optimized to etch through the carbon doped oxide layer and the second etch chemistry is optimized to etch through the silicon dioxide layer.

Regarding **claim 9**, **Aoi** discloses a method for making a dielectric structure for dual-damascene applications as recited in claim 8, wherein, the second etch chemistry is selective to the barrier layer **352** as shown in Fig. 16(d) and 17(a); col. 20, lines 3-13).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoi** in view of **Jang**, as applied to claims **1**, 4, and 33 above and further in view of US 6,043,167 (**Lee** et al.).

The prior art of **Aoi**, as explained above, discloses each of the claimed features except for indicating the low-dielectric constant, carbon-doped oxide layer has a dielectric constant layer of about and no greater than 3.0.

Lee teaches a method of forming a carbon-doped silicon oxide film for use as intermetal dielectrics which can have a dielectric constant of no more than 3.0, as shown in Fig. 2 (col. 1, lines 8-12).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the carbon-doped silicon oxide film having a dielectric constant of no more than 3.0 of

Lee as the carbon-dope silicon oxide film of **Aoi**, because **Aoi** suggests using a low-dielectric constant, carbon-doped silicon oxide layer, and **Lee** teaches such a layer for interlayer dielectrics having a low dielectric constant that reduces RC delay ("crosstalk") and additionally confers the benefits of low internal stress (paragraph bridging cols. 2-3). Moreover, it is a goal of the semiconductor industry to minimize RC delay and thereby speed up chip speeds, such that one of ordinary skill is always motivated to reduce the dielectric constant as far as possible.

Response to Arguments

7. Applicant's arguments filed 29 April 2005 have been fully considered but they are not persuasive.

Applicant argues that because the instant claim 1 is limited by "consisting of" language to limit the features and steps of forming the inter-metal dielectric layer, that Aoi fails to teach each of the claimed features of the instant claims. Examiner respectfully disagrees. Examiner notes with interest that Applicant fails to address what extra features have been included in Aoi that are somehow excluded by the "consisting of" language. As a matter of fact, Aoi presents no extra features excluded by the "consisting of" language of the claims. The elements and steps are exactly as claimed with no extra intervening steps or elements. For example, the carbon doped oxide 354 is formed directly over and in contact with the underlying silicon oxide layer 353. The trench 360, 362, is formed in the carbon doped oxide layer 354 and the via 361 is formed from within the trench 360, 362. Accordingly, the argument is not found persuasive and the rejection over Aoi stands.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached from 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
July 6, 2005